Listing Of Claims

Claims 1-55 (Canceled)

56. (previously presented) A method for testing semiconductor components on a substrate comprising:

providing a switching network;

applying test signals through the switching network to the components on the substrate; and

controlling the test signals using the switching network to perform a selected test on each component on the substrate.

57. (previously presented) The method of claim 56 wherein the selected test comprises functionality testing.

58. (previously presented) The method of claim 56 wherein the selected test comprises parametric testing.

59. (previously presented) The method of claim 56 wherein the selected test comprises burn-in testing.

60. (previously presented) The method of claim 56 wherein the substrate comprises a wafer and the components comprise semiconductor dice.

61. (previously presented) The method of claim 56 wherein the substrate comprises a panel and the components comprise semiconductor packages.

62. (previously presented) The method of claim 56 wherein the substrate comprises a leadframe and the components comprise semiconductor packages.

63. (previously presented) A method for testing semiconductor components on a substrate comprising:

providing a switching network;

applying burn-in test signals through the switching network to the components on the substrate; and

electrically isolating at least one component on the substrate during the applying step using the switching network.

64. (previously presented) The method of claim 63 wherein the applying step is performed using a carrier.

65. (previously presented) The method of claim 64 wherein the substrate comprises a panel and the carrier configured to hold the panel in a burn-in oven.

66. (previously presented) The method of claim 64 wherein the substrate comprises a leadframe and the carrier is configured to hold the leadframe in a burn-in oven.

67. (previously presented) The method of claim 64 wherein the switching network is contained on an interconnect in the carrier configured to electrically engage the components.

68. (previously presented) The method of claim 67 wherein the switching network comprises a die or active electrical switching devices on the interconnect.

69. (previously presented) The method of claim 63 further comprising applying parametric test signals through the switching network prior to the electrically isolating step.

70. (previously presented) A method for testing semiconductor components on a substrate comprising:

providing a carrier configured to hold the substrate;

providing a switching network on the carrier;

applying test signals through the switching network to the components; and

controlling the test signals using the switching network to perform a selected test on the components.

71. (previously presented) The method of claim 70 wherein the carrier includes an interconnect for electrically engaging the components and the switching network is contained on the interconnect.

72. (previously presented) The method of claim 70 wherein the test signals are configured to perform functionality testing of the components.

73. (previously presented) The method of claim 70 wherein the test signals are configured to perform burn-in testing of the components.

74. (previously presented) The method of claim 70 wherein the test signals are configured to perform functionality testing and burn-in testing of the components.

75. (previously presented) The method of claim 70 wherein the substrate comprises a wafer, a panel, a leadframe or a module.

76. (previously presented) The method of claim 70 wherein the switching network comprises a die on the carrier.

77. (previously presented) A system for testing semiconductor components on a substrate comprising:

a carrier configured to hold the substrate;

an interconnect on the carrier configured to electrically engage the components held by the carrier; and

a switching network on the carrier configured to selectively control applying of test signals through the interconnect to the components.

78. (previously presented) The system of claim 77 wherein the substrate comprises a wafer, a panel, a leadframe or a module.

79. (previously presented) The system of claim 77 wherein the carrier comprises a base for mounting the interconnect, a cover for holding the substrate, and a force applying mechanism for biasing the substrate and the interconnect together.

80. (previously presented) The system of claim 77 wherein the carrier comprises an alignment member configured to align the substrate on the carrier.

81. (previously presented) The system of claim 77 wherein the substrate comprises a wafer and the components comprise semiconductor dice.

82. (previously presented) The system of claim 77 wherein the substrate comprises a panel and the components comprise semiconductor packages.

83. (previously presented) The system of claim 77 wherein the substrate comprises a leadframe and the components comprise semiconductor packages.

84. (previously presented) The system of claim 77 wherein the carrier is configured for placement in a burn-in oven and the test signals include burn in test signals.

85. (previously presented) A system for testing semiconductor components on a substrate comprising:

a testing apparatus comprising an interconnect configured to electrically engage the components on the substrate;

a tester in electrical communication with the interconnect configured to generate and analyze test signals for testing the components; and

a switching network on the testing apparatus in electrical communication with the interconnect configured to control test signals applied through the interconnect to the components.

86. (previously presented) The system of claim 85 wherein the testing apparatus comprises a wafer prober.

87. (previously presented) The system of claim 85 wherein the testing apparatus comprises a carrier configured to hold the substrate.

88. (previously presented) The system of claim 85 wherein the testing apparatus comprises a tester and the switching network is configured to expand resources of the tester by transmitting read test signals from selected groups of components.

89. (previously presented) The system of claim 85 wherein the switching network comprises a plurality of active electrical switching devices.

90. (previously presented) The system of claim 85 wherein the substrate comprises a wafer and the components comprise dice on the wafer.

91. (previously presented) The system of claim 85 wherein the substrate compress a leadframe and the components comprise packages on the leadframe.

92. (previously presented) The system of claim 85 wherein the substrate comprises a panel and the components comprise packages on the panel.

93. (previously presented) A system for testing semiconductor components on a substrate comprising:

an interconnect comprising a plurality of interconnect contacts configured to electrically engage the components;

a switching network in electrical communication with the interconnect contacts;

a tester configured to transmit test signals through the switching network and the interconnect to the components;

the switching network configured to multiply and selectively transmit the test signals, to electrically isolate non-functional components and to read test signals from selected groups of components.

94. (previously presented) The system of claim 93 further comprising a carrier containing the interconnect configured to hold the substrate.

95. (previously presented) The system of claim 94 wherein the carrier is configured for placement in a burn-in oven.

96. (previously presented) The system of claim 93 wherein the switching network comprises a die on the interconnect.

97. (previously presented) The system of claim 93 wherein the interconnect comprises a semiconductor material

and the switching network comprises active electrical devices in the material.

98. (previously presented) The system of claim 93 wherein the components comprise dice and the substrate comprises a wafer.

99. (previously presented) The system of claim 93 wherein the components comprise packages and the substrate comprises a leadframe or a panel.

100. (previously presented) The system of claim 95 further comprising a wafer prober containing the interconnect configured to handle the substrate.